

CLAIMS:

1. Apparatus for distributing ADSL signals to customer premises from a central office, comprising:

a central office;

5 the central office having a POTS switching system;

the central office having ADSL connection terminals that connect to a data network;

a plurality of customer locations at least some of which have at least one voice frequency POTS terminal and at least one ADSL terminal;

10 a field cabinet associated with the plurality of customers;

a plurality of individual metallic telephone lines each extending from a respective one of the customers to the field cabinet;

a trunk cable containing a large number of metallic telephone lines and extending from the field cabinet to the central office;

15 the field cabinet including a plurality of connections for connecting the individual telephone lines to the trunk cable for connection of signals between the customer locations and the central office;

the individual metallic telephone lines each being arranged to transmit both voice frequency POTS signals and ADSL signals between the respective
20 customer location and the field cabinet;

a bi-directional link separate from the trunk cable for the transmission of ADSL signals between the field cabinet and the central office for connection to the data network; and

instead, each of the system's two field programmable gate arrays (FPGA) need only one framing channel.

5. The apparatus according to Claim 4 wherein only two of 32 channels contain the framing information.

5 6. The apparatus according to Claim 3 wherein once each ADSL symbol period (250 us), the least significant bit (LSB) of one channel's digital sample carries embedded framing information and in each symbol period, the digital value of this bit is overridden by the current value of a known pseudo random bit stream (PRBS).

10 7. The apparatus according to Claim 6 wherein the interface units are arranged to provide a maximal length sequence with a 15 bit period using a four bit linear feedback shift register (LFSR).

15 8. The apparatus according to Claim 3 wherein two independent sequences are used (one for each FPGA) and the same sequence is used for both upstream and downstream directions of a particular channel, where the sequences are defined by the following equations: $X_0 = X_3 \text{ XNOR } X_4$, and $X_0 = X_1 \text{ XNOR } X_4$ and both sequences are seeded with all zeros.

20 9. The apparatus according to Claim 3 wherein the receiving end discriminates against invalid sequences by monitoring the a moving window of the four most recent bits of the bit stream and the discriminator tolerates no more than one bit error in the window and treats the case of two or more errors in the window as a framing error and therefore take corrective measures.

10. The apparatus according to Claim 1 wherein the interface units are arranged to use fixed gains (unity) for both downstream and upstream paths.

11. The apparatus according to Claim 1 wherein the interface units include Gigabit Ethernet (IEEE 802.3 compliant) laser transceiver modules, 5 serializer-deserializers (SERDES), as well as ADSL coder-decoders (CODEC) and line drivers/receivers.

12. The apparatus according to Claim 1 wherein there is provided a plurality of interface units at the telephone central office each of which the bi-directional link associated with a respective individual telephone line and each of 10 which provides an interface between the respective ADSL signals on the bi-directional link and the ADSL terminal of the central office.

13. The apparatus according to Claim 1 wherein each interface unit includes an analog front end unit for converting between analog signals transmitted to and received from the individual telephone line and digital signals for transmission 15 on and receipt from the bi-directional link,

14. The apparatus according to Claim 13 wherein the analog front end generates parallel data and wherein there is provided interface components for converting between the parallel data and a serial digital signal for communication on the bi-directional link.

20 15. The apparatus according to Claim 14 wherein the analog front end comprises an ADSL codec and filter.

16. The apparatus according to Claim 14 wherein the interface components include a serializer/de-serializer unit arranged to receive the parallel

digitized ADSL signals and serialize them onto a single bit stream and to receive a serial bit stream and generates therefrom parallel data.

17. The apparatus according to Claim 11 wherein serializer/de-serializer also is arranged such that if frame synchronization is lost, then the communication link is recreated by a protocol, whereby if a transceiver loses frame synchronization, it simply ceases transmission to the other transceiver, then the other transceiver will receive idle characters, signaling it to restart transmission and such that once the original transceiver detects frame synchronization, it will begin transmitting data again, and the link will be re-established.

18. The apparatus according to Claim 1 wherein there is provided a power supply unit arranged to receive power from each subscriber premises to power its own channel over the tip and ring phone line.

19. The apparatus according to Claim 1 wherein there is provided a power supply unit arranged to receive power from the central office to power the parts of the interface unit common to all channels.

20. The apparatus according to Claim 19 wherein the power supply unit is arranged to receive power from the central office by two tip and ring lines.